--20. A semiconductor memory device as claimed in claim 1, further comprising:

a connecting portion, provided above each memory cell in the memory blocks, for connecting metallic wiring layers.

--21. A semiconductor memory device as claimed in claim 20, wherein the connecting portion is provided for connecting each column selecting signal line to a sense amplifier for sensing the memory cell.

--22. A semiconductor memory device as claimed in claim 1, wherein:

the target memory cell in the memory blocks is accessed via input/output lines; and

the column selecting signal lines and the input/output lines are arranged perpendicular to each other.--

Please charge the fee of $36 for the addition of two claims of any type in excess of the 20 originally paid for to Deposit Account No. 25-0120.

R E M A R K S

The specification and drawings have been amended to make editorial changes therein, bearing in mind the criticisms in the Official Action, to place the application in condition for allowance at the time of the next Official Action.

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Claim 10 was rejected under §112, second paragraph. The claim is correct in that the global input/output lines are perpendicular to the column selecting signal lines. Figure 2 shows column selecting signal lines YSW that extend from the column decoder 33. The global input/output lines extend from lines YSW into the respective sense amplifier area 35 in a direction that is perpendicular to lines YSW. See also, elements 61-0 and 61-1 in Figure 4 and the discussion at page 24, line 22, through page 25, line 9. Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 1-5 were rejected as anticipated by SANO et al. 4,901,285. Reconsideration and withdrawal of the rejection are respectfully requested because SANO et al. Figure 2 discloses that the word lines driven by the row selecting signal and column selecting signal lines are not parallel to each other.

Figures 1A-B of SANO et al. are merely symbolic representations (column 2, line 55) and do not show the actual device. Thus, even though Figures 1A-B would appear to disclose that the word lines driven by the row selecting signal and column selecting signal lines are parallel to each other, the artisan would recognize that these figures are only symbolic. They do not suggest the claimed arrangement to one of skill in the art. The artisan would look to the actual layout in Figure 2 for guidance how to make the device in SANO

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et al. Figure 2 shows the actual device in which the respective lines are clearly not parallel to each other. The source lines SL run horizontally across the page (perpendicular to the bit lines BL) but the word lines RL take a zigzag path that is not horizontal across the page and thus not parallel to the source lines in plan view. Accordingly, it is believed that claims 1-5 avoid the rejection under §102.

In addition, claim 4 provides that the word lines and the column selecting signal lines are in the same wiring layer. As is apparent from Figure 3, SANO et al. the word lines RL and the signal lines SL are in different wiring layers. Claim 4 avoids the rejection for this additional reason.

Claims 6-7 and 10-13 were rejected as anticipated by SUGIBAYASHI et al. 5,406,526.

Claim 6 has been amended and is believed to avoid this rejection. The reference does not disclose the newly-added column decoding section definition and the word lines set forth in the claim.

Claim 10 provides that the column selecting signal lines and the input/output lines are perpendicular to each other. The Official Action points to Figure 10B in SUGIBAYASHI et al. as disclosing vertical column selecting signal lines and horizontal I/O lines. The horizontal I/O lines are not seen in this figure. The horizontal lines are

main word lines (MWL) and sub word lines (SW). Reconsideration and withdrawal of the rejection of claim 10 are respectfully requested.

Claims 11-12 provide that the sense amplifiers are in an area between lines for outputting the 2-party column pre-decoded signals. As best understood, SUGIBAYASHI et al. do not disclose this feature. The sense amplifiers 41 may be arranged between auxiliary row address pre-decoded signals (Figure 10B of SUGIBAYASHI et al.), but they do not appear to be in an area between lines for outputting the 2-party column pre-decoded signals.

By way of further explanation, the column decoding section performs the main (i.e., final) decoding operation of the column address based on the 2-party column per-decoded signals, so as to select a sense amplifier, where the column decoding section is provided in an area of the memory block where the sense amplifier is provided. In the embodiment as shown in Fig. 9, transistors 110 to 113 function as the column decoding section, and digit lines D and DB are respectively connected with signal lines (i.e., I/O lines) I/OT and I/ON via these transistors, where a sense amplifier is connected to the digit lines D and DB, so as to amplify signals transmitting through these digit lines. That is, both of the 2-party column pre-decoded signals are processed in an area of the memory block where the relevant sense amplifier is provided.

In contrast, in Sugibayashi et al., a plurality of sense amplifiers are selected by using one of 2-party column pre-decoded signals, and a plurality of I/O lines corresponding to the selected sense amplifiers are selected by the other of the 2-party column pre-decoded signals. That is, the area where the one of the 2-party column pre-decoded signals is processed differs from the area where the other is processed (i.e., the other of the 2-party column pre-decoded signals is not processed in an area of the memory block where the sense amplifier is provided), and thus the structure and function are different from those of the present invention. Reconsideration and withdrawal of the rejection of claims 11-12 are respectfully requested.

Claims 8 and 9 were rejected as anticipated by HARIMA 5,468,985. Claim 8 has been amended and reconsideration of the rejection is respectfully requested.

New claims 14-19 are directed to an embodiment of the present invention in which the memory device is a DRAM. In contrast, SANO et al. relates to a read-only memory. The structure disclosed in SANO et al. cannot be applied to DRAMs because the disclosed memory cell structure is particularly complicated and unsuitable for DRAMs.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been

placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Respectfully submitted,

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